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EXAMINER

TSAL, HENRY

ART UNIT PAPER NUMBER

2183

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/783,771	Applicant(s) BIGBEE ET AL.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6,8-15 and 17-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6,8-15 and 17-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 8/16/04 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "111" (page 6); and "290" (page 15). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to, such as in Fig. 3, precisely show MXCSR MASK; MXCSR; and other details such as reserved area as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets

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in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

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3. The disclosure is objected to because of the following informalities:

Fig. 4 is not mentioned in the "GRIEF DESCRIPTION OF THE FIGURES" and "Detailed Description" of the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claims 2-6, 8, 9, 11-15, 17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, the relationship between "a control register mask" and "a memory image" was not defined. Similar problems exist in the other claim 11. Note based on Fig. 3 (originally mailed 2/14/01), the control register mask (MXCSR_MASK) is within "the memory image (300).

In claim 4, it is not clear, based on the claim language, to have the comparing step since the step of "said saved value being stored within said memory image" is unrelated to the comparing step. It is suggested to have the limitation of "said saved value being stored within said memory image" added to

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claim 3 in order to clarify the comparing step. Similar problems exist in the other claim 13.

In claim 6, line 2-3, "said initializing value" lacks proper antecedent basis since it was not defined. It is suggested to change "said initializing value" to -"said initial value-.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6, 8-15, and 17-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juffa (U.S. Patent No. 6,247,117) (hereafter referred to as Juffa'117) in view of

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Temple (U.S. Patent No. 5,875,342) (hereafter referred to as Temple'342).

Referring to claim 1, Juffa'117 discloses, as claimed, a method comprising: accessing a control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A); adjusting a control value for a control register (262, Flags register, see Fig. 6B) as a function of said control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A) to generate a masked control value (DM value for CF under such as FSCALCHK, and FSIINCHK, see Fig. 9); storing (through the numerous checking instruction to set a flag, see Col. 21, lines 11-14) said masked control value (DM value for CF under such as FSCALCHK, and FSIINCHK, see Fig. 9) into the control register (262, Flags register, see Fig. 6B).

Referring to claim 10, Juffa'117 discloses, as claimed, a machine-readable medium (in the main memory or instruction cache 16, see Fig. 3) having stored thereon a set of instructions said set of instructions, which when executed by a processor, cause said processor to perform a method comprising: accessing a control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A); adjusting a control value for a control register (262, Flags register, see Fig. 6B) as a function of said control register mask (such as DM (denormal maskbit) in

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control register 270, see Fig. 7A) to generate a masked control value (DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9); storing (through the numerous checking instruction, see Col. 21, lines 11-14) said masked control value (DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) into the control register (262, Flags register, see Fig. 6B).

Referring to claim 19, Juffa'117 discloses, as claimed, an apparatus comprising: a control register (262, Flags register, see Fig. 6B) comprising a plurality of bits (such as CF, PF, and ZF bits in Fig. 6B) corresponding to a plurality of functions (note such as: CF is for carry flag; PF is for parity flag; and ZF is for zero flag. Each one provides a specific function, see also Col. 19, lines 25-33); a masking mechanism (inherently existing in the Juffa'117's system) to generate a control register by setting inactive one or more bits (see Fig. 9, last column, CF, PF, and ZF are set inactive by "0") of a control value prior to storage of said one or more bits in the control register (see such as 2nd column in Fig. 9).

As to claims 2 and 11, Juffa'117 also discloses: said accessing comprises writing an initial value (CF value before it is replaced by DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) to at least one address within a memory image (262, Flags register, see Fig. 6B).

As to claims 3 and 12, Juffa'117 also discloses: said accessing further comprises executing a state save operation (inherent step in the Juffa'117's system).

As to claims 4 and 13, Juffa'117 also discloses: said accessing further comprises comparing a saved value (DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) to said initial value (CF value before it is replaced by the DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9), said saved value (DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) being stored within said memory image as a result of said execution of said state save operation (inherent step in the Juffa'117's system). Note as set forth above in 112, 2nd rejection, the comparing step, based on the claimed language, has no relationship with the step of "said saved value being method step limitations to claimed invention.

As to claims 5 and 14, Juffa'117 also discloses: said control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A) comprises a default value ("0" , see Fig. 9) if said saved value is equal to said initial value ("0" , see last column in Fig. 9).

As to claims 6 and 15, Juffa'117 also discloses: said control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A) being set to said saved value if said

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saved value is not equal to said initializing value (note CF value is replaced by the DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9).

As to claims 8 and 17, Juffa'117 also discloses: the save operation is an FXSAVE instruction (note FXSAVE is just an alternative name comparing with that used in Juffa'117's system), and the FXSAVE instruction having an associated target address (certainly a target address is inherently existing in a save operation for a saved destination).

As to claims 9 and 18, Juffa'117 also discloses: the target address being an address within the memory image (262, Flags register, see Fig. 6B).

As to claims 20, Juffa'117 also discloses: a mask storage area (control register 270, see Fig. 7A) to contain a pre-determined mask value (such as IM, DM (denormal maskbit), ZM, OM, UM, or PM see Fig. 7A), said mask value indicating which of said plurality of functions are available.

As to claims 21, Juffa'117 also discloses: said mask storage area (control register 270, see Fig. 7A) may be accessed by performing a state saving operation which saves said mask value (such as IM, DM (denormal maskbit), ZM, OM, UM, or PM see Fig. 7A) to a memory location (see Fig. 9, DM is stored in 7th column).

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As to claims 23, Juffa'117 also discloses: said masking mechanism is a hardware masking mechanism (inherently existing in Juffa'117's system).

As to claims 24, Juffa'117 also discloses: said masking mechanism comprises: a sequence of instruction (saved in the main memory or cache memory of the processor 10, see Fig. 3) to adjust a control value by saving state Information including a control register value to a memory and adjusting said control register value based on a readable mask value read from the processor before restoring the state information; execution hardware to execute the sequence of instructions (see described in claim 1 above).

Referring to claim 25, Juffa'117 discloses, as claimed, a processor (processor 10, see Fig. 3) comprising: a decode unit (such as decode unit 24A, or 20B, or 20C, see Fig. 3); at least one of a plurality of registers (such as 270, control Register, see Fig. 7A, in register file 30, se Fig. 3, see also Column 20, line 6-7), said at least one of a plurality of registers comprising a plurality of bits (such as IM, DM, ZM, OM, UM, and PM bits in Fig. 7A) corresponding to a plurality of functions (note IM, DM, ZM, OM, UM, and PM bits in Fig. 7A each one provides a specific function, see also Col. 19, lines 65 to Column 20, lines 1-7); an execution unit (such as Function units

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24A, 24B, and 24C); an internal bus (38, see Fig. 3), said decoder unit (such as decode unit 24A, or 20B, or 20C, see Fig. 3, said at least one plurality of registers (such as 270, control Register, see Fig. 7A, in register file 30, see Fig. 3, see also Column 20, line 6-7), said at least one execution unit (such as Function units 24A, 24B, and 24C being coupled by said internal bus (38, see Fig. 3).

As to claims 26, Juffa'117 also discloses: in response to said execution unit (such as Function units 24A, 24B, and 24C) executing an instruction, said plurality of bits (such as DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) are written to a mask storage area (262, Flags register, see Fig. 6B and see DM and IM in Fig. 9) .

Juffa'117 discloses the claimed invention except for: the masking mechanism for providing the adjusting comprising performing an AND operation in which said control register mask and said control value are operands (in claims 1, 10, 19, and 25).

Temple'342 discloses a system comprising: the masking mechanism (using the mask register 202 and the AND gate 203 see Fig. 2) for providing the adjusting comprising performing an AND operation (using the AND gate 203 see Fig. 2) in which the control register mask (mask register 202 see Fig. 2) and the

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control value (the value such as 201n inside register 201, see Fig. 2) are operands.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Juffa'117's system to comprise: the masking mechanism for providing the adjusting comprising performing an AND operation in which said control register mask and said control value are operands the Juffa'117's system, as taught by Temple'342, in order to selectively enable or disable the control values in the control register of the Juffa'117's system (see Col. 5, lines 25-27).

As to claims 22, and 27-29, Juffa'117/Temple'342 discloses the claimed invention except for: explicitly defining the state saving operation is an FXSAVE instruction (claims 22 and 27); the at least one of a plurality of registers is an MXCSR register (claim 28); and the at least one mask storage area is an MXCSR MASK field. (claim 29). However, FXSAVE is just an instruction name and MXCSR and MXCSR MASK field are just a register and field name. Juffa'117/Temple'342's system certainly provides the same features as the FXSAVE instruction and MXCSR register and MXCSR MASK field.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Juffa'117/Temple'342's system to comprise: said state saving

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operation is an FXSAVE instruction; said at least one of a plurality of registers is an MXCSR register; and said at least one mask storage area is an MXCSR MASK field since they are just an alternative name comparing with that used by the Juffa'117/Temple'342's system.

Response to Amendment

7. Applicant's arguments mailed 8/16/04 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the drawings, specification, and 35 U.S.C. §112, second paragraph problems, Applicant's response has not completely overcome these objections and rejections.

As set forth in the art rejections above, Juffa'117 and Temple'342 teach the claimed invention.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is

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reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the

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status of this application or proceeding should be directed to the TC 2100 receptionist whose telephone number is (703) 305-3900.

10. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306**. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI
PRIMARY EXAMINER

October 16, 2004